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APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: System Architecture and Method for Three-Dimensional Memory

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System Architecture and Method for Three-Dimensional Memory

Cross-Reference to Related Application

This application claims the benefit of U.S. provisional application no. 60/446,910, filed February 11, 2003, which is hereby incorporated by reference.

The following 23 documents are hereby incorporated by reference:

1. "512Mb PROM with 8 Layers of Antifuse/Diode Cells" (to be presented as ISSCC 2003/Session 16/Non-Volatile Memory/Paper 16.4 at the 2003 IEEE International Solid-State Circuits Conference (3 pages)).

2. 23 pages of slides (first slide labeled "Agenda;" last slide labeled "Summary").

3. U.S. Patent No. 6,034,882 to Johnson et al. ("Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication").

4. U.S. Patent No. 6,420,215 to Knall et al. ("Three Dimensional Memory Array and Method of Fabrication").

5. U.S. Patent Application Serial No. 09/928,536 to Johnson ("Vertically-Stacked, Field Programmable, Nonvolatile Memory and Method of Fabrication").

6. U.S. Patent Application Serial No. 10/185,507 to Vyvoda et al. ("Electrically Isolated Pillars in Active Devices").

7. U.S. Patent Application Serial No. 10/326,470 to Herner et al. ("An Improved Method for Making High-Density Nonvolatile Memory").

8. U.S. Patent Application Serial No. 09/748,589 to March et al. ("Memory Devices and Methods for Use Therewith").

9. U.S. Patent Application Publication No. US 2002-0081782 A1 ("Contact and Via Structure and Method of Fabrication").

10. U.S. Patent Application Publication No. US 2002-0136076 A1 ("Memory Device and Method for Sensing while Programming a Non-Volatile Memory Cell").

11. U.S. Patent Application Publication No. US 2002-0136045 A1 ("Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern under a Plurality of Memory Arrays").

12. U.S. Patent Application Serial No. 10/024,647 ("Memory Device and Method for Storing Bits in Non-Adjacent Storage Locations in a Memory Array").

13. U.S. Patent Application Serial No. 10/024,646 ("Memory Device and Method for Redundancy/Self-Repair").

14. U.S. Patent Application Publication No. US 2002-0083390 A1 ("Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein").

15. U.S. Patent No. 6,486,728 to Kleveland ("Multi-Stage Charge Pump").

16. U.S. Patent No. 6,385,074 to Johnson et al. ("Integrated Circuit Structure Including Three-Dimensional Memory Array").

17. U.S. Patent Application Serial No. 09/748,649 to Scheuerlein et al. ("Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operation").

18. (a) U.S. Patent Application Publication No. US 2002-0136047A1 to Scheuerlein ("Method and Apparatus for Biasing Selected and Unselected Array Lines when Writing the Memory Array"). (b) U.S. Patent No. 6,504,753, which has the same specification (excluding the claims).

19. (a) U.S. Patent Application Serial No. 09/896,468 to Scheuerlein ("Current Sensing Method and Apparatus Particularly Useful for a Memory Array of Cells Having Diode-Like Characteristics"). (b) U.S. Patent Application Serial No. 09/897,704 to Scheuerlein ("Memory Array Incorporating Noise Detection Line"), which has the same specification (excluding the claims).

20. U.S. Patent No. 6,407,953 to Cleeves et al. ("Memory Array Organization and Related Test Method Particular Well Siuted for Integrated Circuits Having Write Once Memory Arrays").

21. U.S. Patent No. 6,515,904 to Moore et al. ("Method and System for Increasing Programming Bandwidth in a Non-Volatile Memory Device").

22. U.S. Patent Application Serial No. 10/306,887 to Scheuerlein et al. ("Multiheaded Decoder Structure Utilizing Memory Array Line Driver with Dual Purpose Driver Device ").

23. U.S. Patent Application Serial No. 10/217,182 to Kleveland et al. ("A Dynamic Sub Array Group Selection Scheme").

This invention is directed to a chip-level architecture used in combination with a monolithic three-dimensional write-once memory array. For example, the architecture can be used with any of such memory devices taught in document numbers 3 through 7 in the above list.

The Chip Block Diagram in the above-listed document number 2 exemplifies a preferred embodiment of the architecture showing the functional organization of:

an Error Checking & Correction Circuit (ECC) described in documents 8, 13, and 14 above;

a Checkerboard Memory Array described in document 11 above;

a Smart Write Controller described in documents 10, 13, and 21 above;

a Charge Pump exemplified in documents 15 and 16 above;

a Vread Generator exemplified in document 2 above with a circuit schematic;

an Oscillator;

a Band Gap Reference Generator (precision reference generator); and

a Page Register/Fault Memory described in document 13 above.

Document numbered 17 in the above list shows the user data for one programming request stored temporarily in a register called a page register, programmed into memory cells in multiple sub arrays of the memory device.

Document numbered 18(a) in the above list describes the biasing for selected and unselected array lines of a selected sub array, unselected sub arrays have all their memory

lines held to a common voltage preferably the ground voltage of the chip. Document 18(b) describes a method and apparatus for discharging memory lines of a selected sub array to the voltages required for memory lines in an unselected sub array.

Document numbered 19(a) in the above list describes current sensing method used to sense the state of memory cells on the memory lines of the sub arrays. Document numbered 19(b) in the above list describes a sub array incorporating a noise detection line used in combination with the above sensing method for reliable sensing of small signals from cells in the sub arrays.

The memory device has multiple sub arrays in a checkerboard arrangement. Circuits as described in more detail in document 18(a) are provided that bias the memory lines of selected arrays so they can be accessed for read and write operations, and other circuits as described in document 18(b) that bias the memory lines of unselected arrays so the state of cells in unselected arrays are not disturbed during read or write operations. By these means, the power dissipation of the memory device is much lower than if all cells in the memory were biased for selectivity. The number of selected sub arrays can be modified by control circuits on the memory as described in document 23 in the above list.

The sub arrays have read and write sensing circuitry connected to array lines in one direction (i.e., sensing lines). The circuitry is shared between adjacent subarrays by the method described for checkerboard arrays. The circuitry uses current sensing methods and noise cancellation lines described in documents 18 and 19, particularly the sensing circuit shown in the Read Sense Amplifier figure of document 2 and described in document 1, to allow large sub arrays with reliable sensing. All the sensing circuits for subarrays in a column are connected together by means of shared bi-directional data busses and control lines on a layer of interconnection metal above the memory cells. The data busses and control lines are preferably substantially parallel to one another and parallel to the sensing lines in the memory array. They connect the sub arrays to control circuitry in the smart write controller. The data bus is bi-directionally controlled in both read and write operations to reduce the number of wires required. The smart write controller transfers data between the selected memory sub arrays and a register called a page register/ fault memory during read and write operations. Thereby, the data from the

page register is written to or read from a set of cells distributed across all the selected sub arrays.

The selected sub arrays are preferably all in a horizontal group called a stripe and within the sub arrays the selected cells are preferably all in a single row, i.e., the row decoders in each of the selected sub arrays are coordinated. One of the sub arrays contains the calculated bits for ECC protection of the data as described in document 14. Two other sub arrays located at the left and right ends of the horizontal stripe, and preferably smaller than the user data subarrays, contains supplemental data including flags and other redundancy control bits that thereby can be located in the same single row with the user data. Preferably, each row contains the page register data, as well as ECC data and redundancy control bits. The spreading of the data to many sub arrays improves the effectiveness of the ECC and the coordination of the row decoders facilitates a self-repair mechanism further described in document 13.

The smart write control circuitry achieves variable bandwidth transfers to the sub arrays as described in document 17 and 23. The smart write control circuitry also collects detected errors during programming using the method described in document 10 and steers them to the fault memory portion of the register to activate the self repair mechanism which will reprogram the data from the page register in a row of redundant cells preferably in the same set of selected sub arrays.

The exemplary Vread Generator provides a voltage to which a selected word line is driven during a read operation. Pairs of transistors, labeled N3, per collection of sub-arrays are preferably spatially distributed throughout the die to achieve reduced voltage drop along the reference node Vread. This Vread generator, which provides a voltage to which a word line is driven in a 3-D array, having a distributed portion and a localized portion, can be used alone or in combination with any other elements disclosed herein. It is further described in document number 1 in the above-identified list.

Each memory line has two control transistors, as shown in document 2, the foil titled, "Die Organization 2/3." These are the "two transistors" referred to in the "Tile Organizaton" foil of document 2, while "epsilon" is the amortized cost of the row

decoders and bias circuits. This die organization can be used alone or in combination with any other elements disclosed herein.

Other combinations of particular interest include, as examples, 3-Dimensional Memory with:

1. Smart write controller and oscillator.
2. Smart write controller, a collection of memory subarrays, and a bi-directional connection between the memory subarrays and the smart write controller.
    a. Where in a preferred embodiment, during a write operation, information is transferred bi-directionally, specifically, data is transferred to the subarray for programming cells in the subarray and programming success is indicated to the smart write controller on the bi-directional connection.
3. Smart write and checkerboard.
    a. Where in a preferred embodiment, wiring above memory cells connects the subarrays to the write controller.
    b. Where in a preferred embodiment, a bi-directional connection is used between the memory subarrays and the smart write controller.
4. Set of selected subarrays containing the combination of user data, ECC data, and reducndancy control bits
5. Checkerboard and ECC.
6. ECC and smart write.
7. ECC and on-the-fly redundancy.
8. Vread generator with distributed output.
9. Smart write plus dummy bit lines.
10. Data from the page register is distributed in a corresponding physical row in each of the subarrays
    a. Preferably, each row contains the page register data, as well as ECC data and redundancy control bits.

11. Die organization having two control (driver) transistors per memory line, plus row decoders and bias circuits that are shared amongst memory lines, details of which are provided in document numbered 22 above, optionally in combination with smart write.

Any term, concept, feature, drawing, method, apparatus, system, etc. or portion thereof, described in the above-listed documents can be used alone or in combination to support claims of this or any other non-provisional patent application(s) claiming the benefit of U.S. provisional application no. 60/446,910. Additionally, the material described in the above-listed documents provides only some of many possible implementations. For this reason, the above-listed documents are intended by way of illustration and not by way of limitation. It is only the claims, including all equivalents, in this and any other non-provisional patent application(s) that claim the benefit of U.S. provisional application no. 60/446,910 that are intended to define the scope of inventions supported by the above-listed documents. The following claims express the statements made in this paragraph.